## **CLAIMS**

## What is claimed is:

1	1. An integrated circuit (IC) comprising:			
2	a clock distribution grid distributing a clock to	o local circuits, said distribution grid		
3	having a known load capacitance;	having a known load capacitance;		
4	a clock driver driving said clock distribution g	grid;		
5	at least one inductor connected at one end to s	aid distribution grid, said clock		
6	having a frequency within the frequency range of the	resonant frequency of local grid		
7	capacitance and said at least one connected inductor; and			
8	a power grid, power grid lines being discontin	nuous in the vicinity of each said at		
9	least one inductor, whereby power grid line loops are open in the vicinity of each said at			
10	least one inductor.			
1	2. An IC as in claim 1, wherein said at least one	inductor is connected to a		
2	decoupling capacitor (decap) at an other end.			
1	3. An IC as in claim 2, wherein a voltage develo	ps across each said decap, said		
2	voltage being midway between a high level and low level of said clock.			
1	4. An IC as in claim 3, wherein said decap is a p	air of decaps, a first of said pair		
2	being connected between a first supply line and said of	other end of said inductor and an		
3	other of said pair being connected between said other	end and a second supply line.		
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i	5. An IC as in claim 4, wherein said second supp	oly line is a ground line.		
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1	6. An IC as in claim 1, wherein said power grid	lines include supply and supply		
2	return lines terminating on endpoints.			

1	7.	An IC as in claim 1, wherein said at least one inductor is four inductors located in		
2	four o	four quadrants around said clock driver.		
1	8.	An integrated circuit (IC) comprising:		
2		a clock distribution grid distributing a clock to local circuits, said distribution grid		
3	havin	having a known load capacitance;		
4		a clock driver driving a first clock phase in said clock distribution grid;		
5	at lea	at least one inductor connected at one end to said first clock phase, said clock having a		
6	frequ	frequency within the frequency range of the resonant frequency of local grid capacitance		
7	and s	and said at least one connected inductor; and		
8		a second clock phase, said at least one inductor being connected to said second		
9	phase	phase at an other end, said local grid capacitance comprising local wiring capacitance		
10	from	from both of said first clock phase and said second clock phase.		
1	9.	An IC as in claim 8, further comprising:		
2		a pair of cross coupled inverters connected between said first clock phase and said		
3	secon	d clock phase.		
1	10.	An IC as in claim 8, further comprising a second clock driver driving said second		
2	clock	phase.		
1	11.	An IC as in claim 8, wherein said at least one inductor is four inductors located in		
2	four o	quadrants around said clock driver.		
1	12.	An integrated circuit (IC) assembly clocked by a global clock, said global clock		
2	being	distributed to a plurality of sectors, each of said sectors comprising:		
3		a clock distribution grid distributing a sector clock to local circuits, said		
4	distri	distribution grid having a known load capacitance;		
5		a clock driver driving said clock distribution grid;		

6		at least one inductor connected at one end to said distribution grid, said clock		
7	havin	having a frequency within the frequency range of the resonant frequency of local grid		
8	capac	capacitance and said at least one connected inductor; and		
9 .	•	a power grid, power grid lines being discontinuous in the vicinity of each said at		
10	least o	least one inductor, whereby power grid line loops are open in the vicinity of each said at		
11	least (	least one inductor.		
1	13.	An IC assembly as in claim 12, wherein said at least one inductor is connected to		
2	a dece	a decoupling capacitor (decap) at an other end.		
1	14.	An IC assembly as in claim 13, wherein a voltage develops across each said		
2	decap	, said voltage being midway between a high level and low of said clock.		
1	15.	An IC assembly as in claim 14, wherein said decap is a pair of decaps, a first of		
2	said p	pair being connected between a first supply line and said other end of said inductor		
3	and a	and an other of said pair being connected between said other end and a second supply		
4	line.			
1	16.	An IC assembly as in claim 15, wherein said second supply line is a ground line.		
1	17.	An IC assembly as in claim 12, wherein said clock driver is driving a first clock		
2	phase	phase, said one end of said at least one inductor being connected to said first clock phase		
3	said I	said IC further comprising:		

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a second clock phase, said at least one inductor being connected to said second

phase at an other end, said local grid capacitance comprising local wiring capacitance

from both of said first clock phase and said second clock phase.

1	10.	An ic assembly as in claim 17, turner comprising.			
2		a pair of cross coupled inverters connected between said first clock phase and said			
3	second clock phase.				
1	19.	An IC assembly as in claim 17, further comprising a second clock driver driving			
2	said :	said second clock phase.			
1	20.	An IC assembly as in claim 12, wherein said at least one inductor is four inductors			
1		·			
2	locat	ed in four quadrants around said clock driver.			
1	21.	An integrated circuit (IC) assembly clocked by a global clock, said global clock			
2	being	being distributed to a plurality of sectors, each of said sectors comprising:			
3		a clock distribution grid distributing clock phases to local circuits, said			
4	distri	distribution grid having a known load capacitance for each of said phases;			
5		a clock driver driving a first phase of said phases; and			
6		at least one inductor connected at one end to said first phase and to said second			
<b>7</b>	phase	e at an other end, said clock having a frequency within the frequency range of the			
8	•	resonant frequency of load capacitance for both of said first phase and said second clock			
9		phase and said at least one.			
1	22.	An IC assembly as in claim 21, further comprising:			
2	•	a power grid, power grid lines being discontinuous in the vicinity of each said at			
3	least	least one inductor.			
	22	An IC consultation of the control of			
1	23.	An IC assembly as in claim 22, wherein said power grid lines include supply and			
2	supp	supply return lines terminating on endpoints, whereby power grid line loops are open in			

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the vicinity of each said at least one inductor.

- 1 24. An IC assembly as in claim 21, further comprising:
- a pair of cross coupled inverters connected between said first clock phase and said
- 3 second clock phase.
- 1 25. An IC assembly as in claim 24, further comprising a second clock driver driving
- 2 said second clock phase.
- 1 26. An IC assembly as in claim 21, wherein said at least one inductor is four inductors
- 2 located in four quadrants around said clock driver.
- 1 27. An IC assembly as in claim 21, wherein said clock grid is on a first IC chip and
- 2 ones of said at least one inductor are on an interposer connected to said first chip.